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☐ 1.   Document ID: US 6470443 B1

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L25: Entry 1 of 2                    File: USPT              Oct 22, 2002
```

US-PAT-NO: 6470443
DOCUMENT-IDENTIFIER: US 6470443 B1

TITLE: Pipelined multi-thread processor selecting thread instruction in inter-stage buffer based on count information

DATE-ISSUED: October 22, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Emer; Joel S.	Acton	MA		
Stamm; Rebecca	Wellesley	MA		
Fossum; Trggve	Northborough	MA		
Halstead, Jr.; Robert H.	Belmont	MA		
Chrysos; George Z.	Marlboro	MA		
Tullsen; Dean	San Diego	CA		
Eggers; Susan	Seattle	WA		
Levy; Henry M.	Seattle	WA		

US-CL-CURRENT: 712/205

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 2.   Document ID: US 6073159 A

```
L25: Entry 2 of 2                    File: USPT              Jun 6, 2000
```

US-PAT-NO: 6073159
DOCUMENT-IDENTIFIER: US 6073159 A

TITLE: Thread properties attribute vector based thread selection in multithreading processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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(L24 AND L18).PGPB,USPT.	2

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